UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
[illegible]	[illegible]	[illegible]	[illegible]

EXAMINER
[illegible]

ART UNIT	PAPER NUMBER
[illegible]	18

DATE MAILED: 6/10/92

[illegible]
[illegible]
[illegible]

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 4/16/92 ☐ This action is made final.

A shortened stetutory period for response to this action is set to expire 3 month(s), _____ days from the dete of thie letter.
Failure to respond within the period for response will ceuse the application to become ebendoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Petent Drawing, PTO-848.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Petent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 7,9-13,15 and 17-70 are pending in the application.

   Of the ebove, claims _____ are withdrewn from consideretion.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ ere ellowed.

4. ☒ Claims 7,9-11,13,15 and 17-70 are rejected.

5. ☒ Claims 12 ere objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This epplication has been filed with informal drewinge under 37 C.F.R. 1.85 which are eccepteble ior examination purposes.

8. ☐ Formal drewings era required in response to this Office ection.

9. ☐ The corrected or substituta drewinge heve been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not ecceptable (see explenation or Notice re Patent Drewing, PTO-948).

10. ☐ The proposed additional or substituta sheet(s) of drawings, filed on _____ has (heve) been ☐ epproved by the exeminer. ☐ disapproved by the exeminar (see explenetion).

11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanetion).

12. ☐ Acknowledgment is meda of the cleim ior priority under U.S.C. 119. The certified copy hes ☐ been received ☐ not been received ☐ been filed in parant applicetion, serial no. _____ ; filed on _____

13. ☐ Since this applicetion appears to be in condition for ellowence excepi for formal metters, prosecution as to the merits is closed in eccordance with the prectica under Ex perte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

1. Claim "1" in the amendment filed on 4/16/92 is apparently claim 7 amended, and accordingly has been renumbered as claim 7.

2. Claims 13, 15, 17-20, 22, 24-33, 43-51, 61, 62, 65, 66 and 69 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, lines 20-21 appear to be redundant with lines 8-9. In claim 20: in line 10, --chip-- is misspelled; in line 14, --means is-- is misspelled. In claim 22, lines 7 and 15, --means-- is misspelled. In claim 24: in lines 13-14, "is applied by" should apparently read as --receives--; in line 15, "flows" should apparently read as --carries--; in line 16, --means is-- is misspelled. In claims 27-30, 32, 33, 61 and 62, "first transistor" should apparently read as "third transistor", in order to be consistent with claims dependent upon 21-23, which recite a "third transistor" in the "reference voltage generating means", and to be consistent with claim 69, which recites a different "first transistor" in the "first circuit".

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 7, 9-11, 13, 15, 17, 18 and 20-70 are rejected under 35 U.S.C. § 103 as being unpatentable over Alaspa.

Alaspa discloses an on-chip power-on reset circuit in MOS technology.
V_{DD} is an "external supply voltage", and V_R is an "internal power supply voltage" because current flows through terminal 52. An "internal power supply means" comprises the channel of transistor 44.

Figure 3 shows the transfer characteristic of V_R/V_{DD}. A "first rate" corresponds to the slope at segment A up to, but not including, the downturn before segment B. A "second rate" corresponds to the slope at the downturn before segment B, which is at a "larger magnitude" of V_R. A "third rate" corresponds to segment C "after" the downturn, providing a precursor to a full operation point on segment D and therefor enabling "testing" of chip logic after reset. A "fourth rate" corresponds to segment D.

Alaspa does not describe "testing" in any detail. At the time the invention was made, it would have been obvious to a person having ordinary skill in the art to test a chip including the reset circuit disclosed by Alaspa, because chip fabrication was typically unreliable.

Regarding claims 9 and 15, circuitry driving the gate of transistor 44 responds to changes in V_{DD}, thereby "detecting" such changes.

Regarding claims 10 and 17, the downturn between segments A and B corresponds to a "normal operation state" because turning a chip off and on is a normal operation. Full operation on segment D provides "aging" over time.

Regarding claims 11 and 18, the slope at segment C is greater than the slope at segment D.

Regarding claims 20 and 21, registers and latches receiving V_R comprise a "second circuit", other chip logic elements comprise a "first circuit" receiving V_{DD}. A voltage reference stage 12 comprises a "reference voltage generating means". In addition to the channel of transistor 44, the "internal power supply means" comprises an amplifier inverter stage 14 and interposed circuitry connected to the gate of transistor 44.

Regarding claim 22, transistor 44 is a "converter transistor". The signal at the gate of transistor 44 is a "reference voltage" because it is constant during full operation of the chip logic at constant V_{DD}.

Regarding claim 23, logic elements such as drivers are typically used as an "interface circuit" in relation to registers and latches that provide an "internal circuit".

Regarding claim 24, registers and latches are a "load circuit" because they receive current through the terminal that provides V_R.

Regarding claims 25, 26, 34, 35, 43, 44, 52 and 53, a diode 20 has a resistance, as does transistor 24 configured as an active resistance.

Regarding claims 27-30, 36-39, 45-48, 54-57 and 61-68, transistor 22 is a "third transistor" that receives a "control signal" from a manual reset input.

Regarding claims 31, 40, 49 and 58, registers and latches are "memory cells".

Regarding claims 32, 33, 41, 42, 50, 51, 59 and 60, MOS transistors have oxide-insulated gates.

5. Claims 69 and 70 are rejected under 35 U.S.C. § 103 as being unpatentable over Alaspa as applied to claims 20 and 23 above, and further in view of Takanishi et al.

At the time the invention was made, it would have been obvious to a person having ordinary skill in the art to provide an "interface circuit" with transistors that have a higher breakdown voltage than that of transistors used for latches and registers on a chip that has the reset circuit disclosed by Alaspa, because Takanishi discloses the desirability of using high breakdown voltage transistors for driving signals off-chip.

6. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 19 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims and to overcome the rejection under 35 U.S.C. § 112.

8. Applicant's arguments filed on 4/16/92 have been fully considered but they are not deemed to be persuasive.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

10. Any inquiry concerning this communication should be directed to Stephen Baker at telephone number (703) 308-0850.

SMB
January 11, 1993

STEPHEN M. BAKER